Investigation into Socketed CDM (SDM) Tester Parasitics

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Abstract - The ESD Association standards working group 5.3.2 is analyzing the procedure and stress that is applied to a device under test (DUT) using a socketed discharge model (SDM) test system, formerly referred to as socketed CDM. Our final goal is to define an SDM tester specification that will guarantee test result reproducibility across different test equipment. This paper investigates the effect of tester background parasitics on the discharge current waveforms of an SDM tester. Characteristic waveforms were studied and SDM testing was performed on actual devices. It is shown that SDM tester parasitics determine the stress applied to the DUT. This directly impacts the SDM failure threshold voltage levels and may lead to miscorrelation and non-reproducibility of test results across different SDM test systems. This paper empirically determines the relative contributions of the various tester parasitics to the total stress applied to the DUT. Our investigations indicate that the tester provides a 10pF to 20pF parasitic capacitance discharge into each pin of the device. Tester background parasitic elements play such an important role in the SDM discharge event that correlation between test systems built by different manufacturers is unlikely without completely duplicating a particular tester.

I. Review: from CDM to SDM

The concept of a Charged Device Model (CDM) event was introduced by Speakman [1] in 1972, but it was not until 1979 that Bossard et al. [2] designed the first test system. This "tester" involved placing a device "dead bug" in intimate contact with a ground plane while charging and discharging through a relay. Since then, others have sought to make a "perfect" tester that would closely reproduce a real-world air-discharge CDM event [3-5]. Avery [3] showed that the relay used by Bossard [2] introduced parasitics into the discharge path, thereby modifying the discharge event. Furthermore, the additional parasitic inductance of the relay and associated wiring made it impossible to determine the relative sensitivity of the same device in different package configurations. Gieser [4], Renninger [5], and others have since worked to further reduce the discharge and current-monitor parasitics to approximate a real-world CDM ESD event. The test results obtained from these test systems were used to produce ESD Association Standard Test Method 5.3.1 for CDM.

The resulting CDM test systems have proved valuable tools for identifying CDM-sensitive semiconductor components and reproducing CDM field-failure signatures. However, these testers proved difficult to use with devices having high pin-counts, small pin pitches (less than 1.5 mm) or needle-like pins. Also, these CDM testers do not allow for in-situ measurement of DUT I-V curves. Consequently, tester manufacturers pursued an alternative approach: place the device under test (DUT) in a socket and integrate the test into existing commercial Human Body Model/Machine Model test systems.

From a theoretical analysis of both test methods, however, it is clear that CDM and SDM are very

different. In the CDM method the stored charge is mainly in the package, between the leadframe and the external ground plane. In small plastic packaged devices, the majority of charge is stored between the chip and/or chip mounting "paddle" and the ground plane, with minor contribution from the leadframe "pins" [3]. However, the location of stored charge differs as the number of pins increases. For very high pin-count packages, most of the energy can be stored on the "pins" rather than the chip mounting "paddle". This sharing of energy storage can also affect the discharge current waveform.

The CDM event consists of several parts. The initial discharge is from the capacitance associated with the lead frame finger of the pin being grounded. This is rapidly followed by the main chip/paddle capacitance and then the remaining leadframe pin fingers. The paths feed discharge current into the chip through their individual connections, producing a combined output current through the grounded discharge pin. These events occur simultaneously, with the current contributions being controlled by the capacitance and series inductance of the device.

The socketed CDM test method basically enhances the package parasitics by placing the device in a socket, mounted on a test fixture board, and connected via pogo pins to a relay switching matrix. Since the device itself is **not** in intimate contact with a ground plane, the stored energy is located on the tester components, associated wiring, and, to a much lesser degree, the device socket. The discharge event is similar to CDM in qualitative sequence (i.e., discharging pin, device, capacitance on other "non-grounded" pins) but is quite different in quantitative terms; the main package storage components are relatively small and the "parasitic" capacitance on the pins due to the tester can be quite large. In fact, it can be large enough that failure can occur at a pin which is not used as a direct discharge pin [11].

For a long time, both test approaches were called Charged Device Model tests. Each was differentiated by denominators such as "robotic" and "socketed", later replaced with "non-socketed" and "socketed". Most recently, the ESD Association standards working group 5.3.2 determined that the test methods would be better distinguished as CDM and SDM (socketed discharge model), since the socketed approach cannot replicate a true charged device model discharge.

Nevertheless, the socketed test method has shown to be reasonably effective in screening out CDM sensitive devices. This occurs despite the fact that the amount and type of stress applied to a DUT in an SDM test is very much dependent upon the test board and tester. In general, the SDM and CDM stress voltage levels cannot be compared, as the discharge current values for each test method are not equal.

Several recent publications have pointed to test result correlation issues [4, 6-11]. Most publications compared data taken on various CDM testers and on a single, very specific commercial SDM tester, but a few papers also collected data on two completely different built socketed tester systems [4, 6, 10]. The findings from these papers showed that there was no correlation of test results between the two different SDM testers. For some devices, the failure mechanism and failure mode were different. For those devices that did show the same failure mode and mechanism, there was no consistent correlation between voltage threshold levels and no consistent discrimination between identical IC's in different package configurations. This clearly indicated that the existing SDM tester specifications were totally inadequate [10].

SDM test system characterization required revision. After using the initial four wire module [ESDA DS5.3-1993] and an intermediate two point probe approach [KT-2 module], the efforts focused on calibrating the test systems using "short modules". These new calibration modules internally short a number of pins together in a socket and allow the insertion of a current probe at one pin. As such, the discharge current of a metal plane, rather than a semiconductor device, can be recorded. In 1994, Verhaege et al. showed that such a discharge event is very representative of the actual SDM stress seen by a DUT [10, 12, 16].

Gieser [4] emulated and studied the principle influences of the parasitics associated with a socketed tester by means of adding discrete transmission lines and background capacitance to a non-socketed air-discharge CDM tester. Serious concerns about the possibility of correlating or unifying the SDM and CDM test methods were raised.

In Section II of this paper, we analyze and develop a basic model of the SDM tester. Section III studies and quantifies the various contributors to the tester background capacitance while also investigating variations between test fixture boards. Section IV examines the effect of coupling capacitance on the discharge event. Section V presents SDM test data obtained from actual integrated circuits. Finally, Section VI summarizes the important conclusions from this work.

II. SDM Tester Model

Figure 1 shows a simplified schematic of the tester background impedance at each socket pin of the SDM test system investigated. The change-over relay normally connects to four reed relays. Hence, the capacitance associated with these four relays (Cp) is connected to the socket pin via a copper trace on the test fixture board (TFB) between the DUT socket and the relay matrix. Each device pin that is inserted into the socket electrically sees this parasitic background capacitance. When energized, the change-over relay contacts to a ground connection and provides a discharge path for the SDM event.

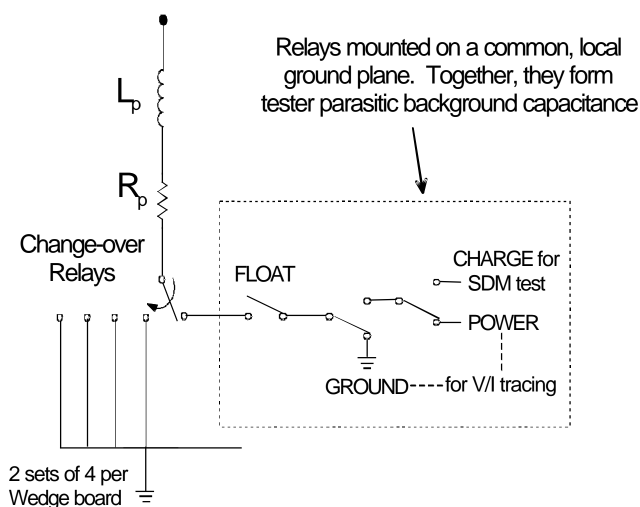

Figure 1: Simple model for the SDM tester parasitic background impedance of each test system socket pin. Each pin has parasitic series inductance (Lp) and resistance (Rp). The change-over relay is used for the SDM discharge.

Figure 2 shows a simplified schematic for a series of "n" socket pins. The four relays per pin are replaced by a lumped capacitor Cp. The series inductance (Lp) and resistance (Rp), in addition to the inductive (Lpp) and capacitive (Cpp) coupling between pins, are shown as well. Although this schematic is very basic, it nevertheless represents a very useful SDM tester model.

Figure 2 also shows the location of a current probe at a designated discharge pin. Both the Tektronix CT-1 and the KT-1 inductive current probes have been used in this work. In addition, Figure 2 includes a schematic representation of a DUT, "short module", or KT-2 module. The latter consists of two pogo pins connected by a wire that is fitted through a KT-1 current probe, with everything mounted on a small PCB board [13] (See figure A5 for a description of the KT-2 module in Appendix II).

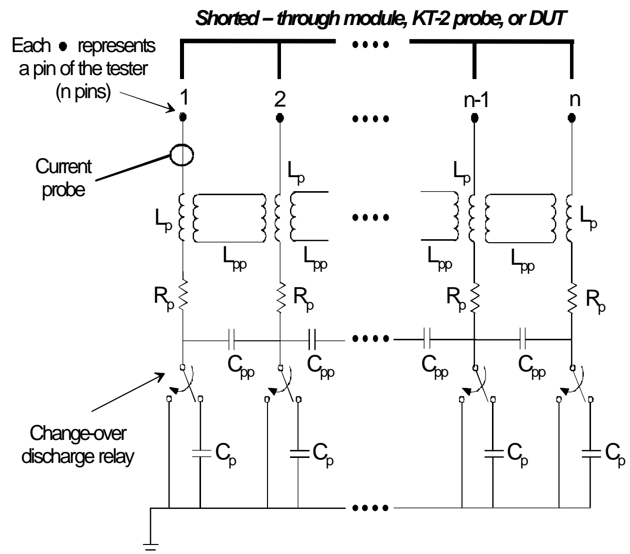

Figure 2: Simple model for "n" socket pins, including capacitive (Cpp) and inductive (Lpp) coupling. The relay background capacitance (illustrated in Figure 1) is replaced by a single lumped capacitor (Cp); one per pin.

Although one pin is designated as the **charge** pin, all "pins" are charged through the short module. This is also true when the short module is replaced by a DUT. After the charge-up sequence of the SDM test occurs, all device pins reach an equal voltage through internal leakage, junction conduction, or junction breakdown. Therefore, the same charge voltage is reached for the internal tester capacitance associated with each DUT pin. Hence, the total charge in the test system includes the charge stored in the device and all of the charge associated with each DUT pins internal tester capacitive and inductive elements, which is illustrated in figure 2. During the discharge event, the total energy that flows through the **discharge** pin includes the energy in the DUT and the energy stored in the capacitance and inductive elements associated with each DUT pin.

In its simplest form, this is somewhat similar to charging a small capacitor and discharging it into the pin of the DUT. This approach to "CDM-like" testing was first introduced by Wada [14] and is known as the small capacitor method (SCM). The differences between the SCM and SDM are as follows. The series inductance is larger in the SDM tester. After charging the DUT, the voltage difference between the small capacitor and the DUT pin is zero. Finally, the capacitor for each pin discharges simultaneously during the SDM event, rather than one pin at a time as proposed in the SCM test.

III. Refining and Quantifying the SDM Tester Parasitics

The detailed construction of the commercial SDM tester investigated is very complex (see Appendix I). We began our investigation into the SDM tester parasitics by first examining the 32 pin TFB in a 256 pin tester.

The socket pin relays are mounted on HV-relay boards (also referred to as wedge cards) in groups of eight. In the 32 pin TFB individual groups of relays are connected to either even or odd socket pins. Connections to the even pins travel on one side of the TFB, while the odd pin connections travel on the opposite side. The trace lines are interdigitated with each other as shown in Figure 3. This leads to complex coupling (both capacitive and inductive) between adjacent lines on opposite sides of the TFB, as well as on the same side of the TFB.

When we examined larger TFBs for the 512 pin test system, however, we found that the coupling becomes even more complex: the TFB is a three layer board and trace lines are not always conveniently run parallel to each other. This alone raises questions about the repeatability of the test using a low pin count TFB/tester compared to the full 512 pin TFB/tester combination, even though both would use the same device socket.

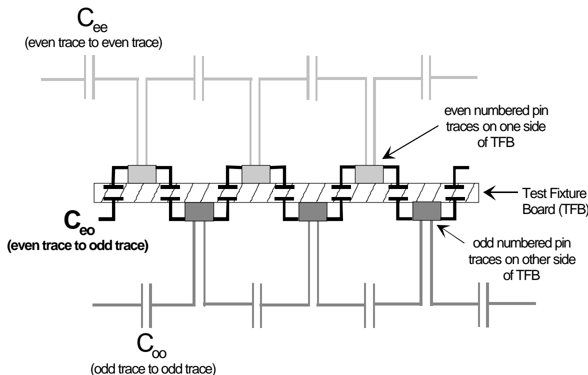

Figure 3 : Interdigitated metal trace lines on a SDM test fixture board create a complex interconnection of the pin-to-pin capacitances: even trace to even trace (Cee), odd trace to odd trace (Coo), and even trace to odd trace (Ceo).

Figure 4 illustrates a more detailed SDM test system model based on the construction of the tester described in Appendix I. This model attempts to separate the various types of parasitics and their locations within the tester: the socket, the metal traces on the test fixture board, the pogo pins, and the relay matrix.

A full analysis of the tester would involve the modeling of coupled transmission lines in the time domain which is beyond the scope of this paper. We adopted a simplified approach, concentrating on measuring pin-to-pin and pin-to-ground capacitance. However, it is clear that the parasitic inductance is **not** insignificant, particularly for the larger pin-count configurations. All capacitance measurements were made at a test frequency of 1 MHz using an HP 4280 capacitance meter.

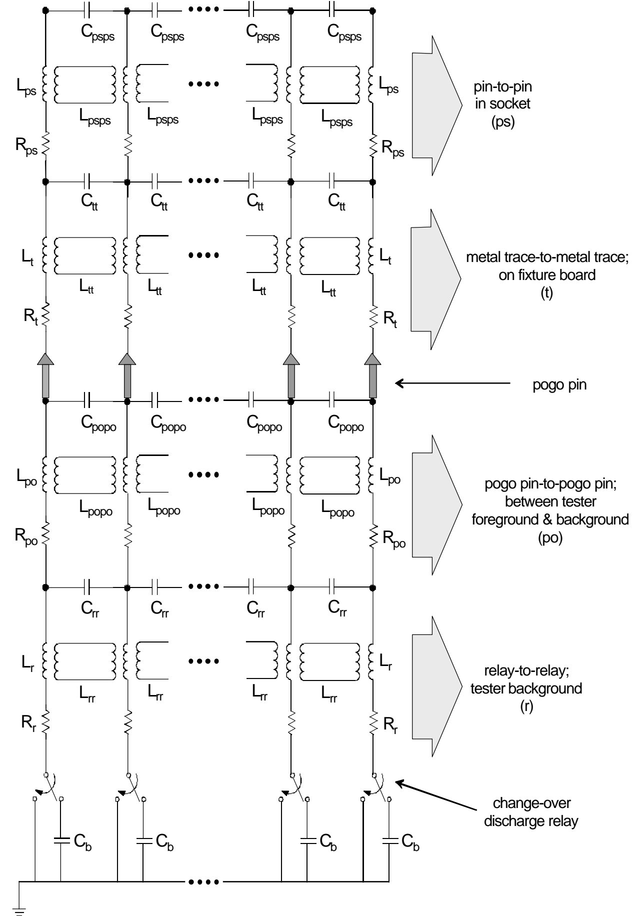

Figure 4: More detailed model of the SDM tester background, which discriminates between different physical locations within the tester.

For a 32 pin TFB with a 32 pin socket, the pin-to-pin capacitance (Cpsps plus Ctt as shown in Figure 4) ranged from 1.0 pF to 1.4 pF. Without the socket, the pin-to-pin capacitance (now simply Ctt) ranged from 0.35 pF to 0.8 pF. The capacitance values between two even or two odd pins ranged from 0.5 pF to 1.0pF with the socket, and from 0.2 pF to 0.6 pF without the socket. These results indicate that capacitance between adjacent trace lines on opposite sides of the TFB is larger than between trace lines on the same side of the TFB. This makes for an even more complex coupling between pins.

The capacitance to ground for several pins was measured

with the TFB mounted in the tester. For the 32 pin TFB, the capacitance to ground ranged from 9.5 pF to 9.9 pF.

Similar measurements were made using the 256 pin PGA TFB and socket. Capacitance values to ground varied from 11.6 pF to 15.7 pF, a significantly wider variation than that seen on the 32 pin TFB. The pin-to-pin capacitance for the 256 pin TFB and socket also showed a wide variation; from 1.4 pF to 6.5 pF. The largest TFB capacitance values were observed between pins that used the same wedge card. The trace lines frequently overlapped each other, probably accounting for the higher pin to pin capacitance.

Testing and analysis using the 512 pin tester has not been completed. Since the 512 pin tester is basically two coupled 256 pin testers, we expect to find even larger capacitance values and wider variations in pin-to-pin capacitance values than that identified for the 256 pin tester. The inductance of the TFB copper trace lines, running between the relay wedge cards and the device socket, are also expected to be much larger.

In a normal situation, with the TFB having the same number of trace lines as DUT pins (i.e., a 32 pin device in a 32 pin socket mounted on a 32 pin TFB), all adjacent pins connected to the device are at the same electrical potential. Therefore, the pin-to-pin capacitance elements (Cpp, Ctt, Cpsps, Crr and Cpopo) can be ignored. If, however, a 14 pin device is inserted into the same 32 pin socket, those pins adjacent to the end pins of the 14 occupied socket pins can contribute to the total charge. Clearly, from the data presented, the capacitance contribution from traces adjacent to end pins on a 32 pin TFB would be significantly different from that seen on a 256 pin TFB.

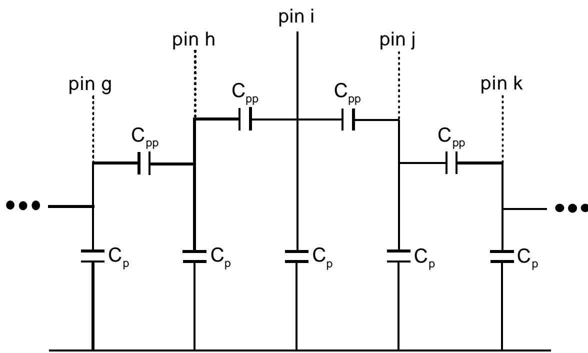

Figure 5: Cascode tree of Cp and Cpp which determines the effective capacitance to ground at a given pin "i".

Figure 5 shows a simplified capacitive coupling "tree" for a single end pin, with adjacent traces "floating". For the 32 pin TFB, Cp is about 10 pF and Cpp about 1.2 pF. This yields an effective end-pin capacitance nearly 20% higher than for a middle pin.

The same analysis for the 256 pin TFB is more complex due to the higher spreads in capacitance values. However, taking average values of 13.5 pF for the pin-to-ground capacitance and 3.5 pF for the pin-to-pin capacitance, the effective end-pin capacitance would increase by nearly 40%.

Since the background capacitance of all of the DUT pins in the tester is so large (10 – 20 pF), a change in the design of a package type for example from PLCC28 to PQFP44 may be insignificant [10]. A small capacitance change in the device from 2.8 pF to 4.4 pF represents a change of only 11% in the SDM test system, but it represents an increase of 157% for the DUT in a CDM test system. Examining these results clearly shows why the SDM tester is unable to detect any difference in fail voltages due to relatively large changes in the package capacitance, but comparatively small changes to the SDM test system capacitance.

IV. Examining the Discharge Event

Discharge waveforms were captured for a 14 pin short module placed in a 32 pin DIL socket TFB mounted on a 256 pin tester. The TFB actually contains eight 32 pin sockets. Socket location #4 was used for this test. Pins 1 to 13 were placed in the socket with pin 14 used to monitor the discharge current. Figure 6 shows the discharge current waveform for a 500 volt charge potential. The same short module was then placed in a 512 pin PGA socket TFB mounted on a 512 pin tester. The same pin connections and charge potential produced the waveform shown in Figure 7. Both waveforms were recorded using the same vertical and horizontal settings.

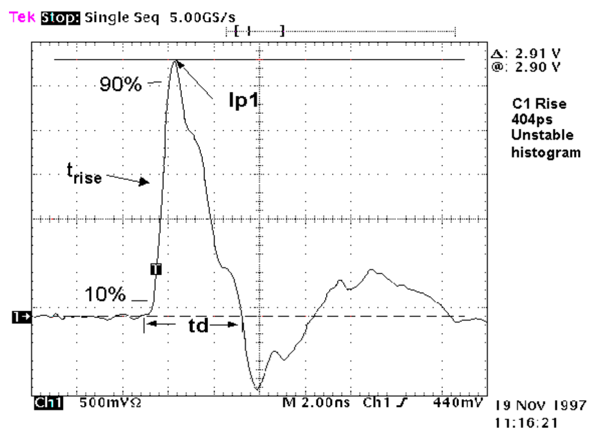

Figure 6: Discharge waveform for a 14 pin short module in a 32 pin TFB mounted on a 256 pin test system.

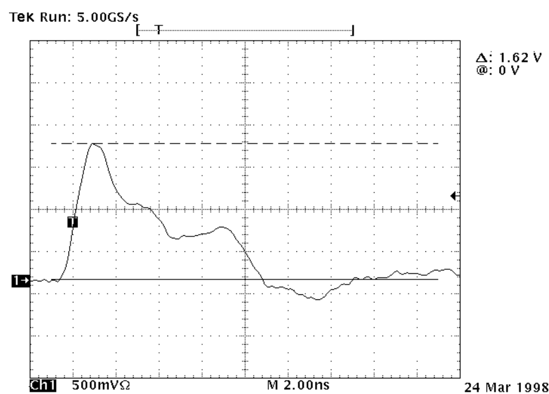

Figure 7: Discharge waveform for a 14 pin short module in a 512 pin TFB mounted on a 512 pin test system.

Figure 7 clearly shows the effect of increased capacitance and inductance for the higher pin-count tester. The pulse period has more than doubled, and the amplitude is roughly 56% of that obtained with the smaller TFB. The pulse rise time has also been affected. This raises some serious concerns:

a) about the significant difference in waveforms between the large and small pin count testers.

b) whether the larger pin-count testers can really provide a CDM-like discharge event.

This data illustrates that a test system using different TF boards will not reproduce the same SDM stress, even if the same device is inserted into an identical socket. A 64 pin device tested using a 64, 128, 192 or 256 pin system will only see the same SDM stress for the same pre-charge voltage, if the traces in TFB are designed the same. In addition, testing devices with less than or equal to 256 pins on a 512 pin system will result in a significantly different SDM stress for the same pre-charge voltage. This data also shows that the same device may give significantly different SDM test results, if the length, width, thickness and layout of the metal trace lines on the TFB are significantly different.

Figure 8 shows the comparison between all pins of the 14 pin short module in the test socket (waveform A), and a two pin short module in the socket (waveform B) (see Figure A4). The charge potential was 1 kV for both cases. Waveform B clearly shows the effects of reduced charge capacitance and increased series inductance. The waveform "structure" (ringing content) is also greater, indicating an increase in the coupling from other components in the tester.

Another interesting fact to note is that the peak current for the "all pin" discharge is not double the peak current for the 500 volt discharge shown in Figure 6, but only about 92% of the expected value. This is due to the "all pin" measurements being performed using socket location #1 on the TFB while the 500 V discharge shown in Figure 6 used socket location #4. Although not sufficient to cause mis-catagorization in most cases, this again shows that differences can occur due to socket location.

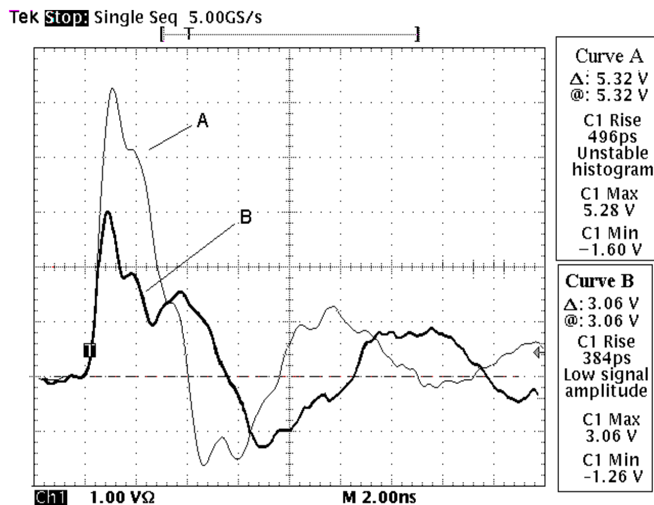

Figure 8: Discharge waveforms for a 14 pin short module. Waveform A = all pins in the test socket; and waveform B = 2-pin short module (module rotated 90 degrees) so that only two pins were in the test socket.

V. SDM Device Testing

SDM testing was performed on two different memory devices. The first device (referred to as Device A) was a 0.8 mm CMOS technology memory device assembled in a 26 pin PSOJ package. The second device (referred to as Device B) was a 0.4 mm CMOS memory device assembled in a 32 pin PLCC package. Both devices were stressed using their respective test fixture boards (TFBs): 28 pin PSOJ and 32 pin PLCC.

Device A was stressed positive from 700V to 1100V in 50V increments. Device B was stressed negative from -800V to -1200V in 50V increments. Previous SDM testing of these devices determined that the most sensitive pins failed within the polarity and stress voltage levels listed.

First, a regular SDM test was performed. For both device types, the Vss pin was designated as the charge pin. In a series of tests, each of the remaining pins were designated, one at a time, as the discharge pin. The results indicated Device A failed at pin 1 with a 800V stress and Device B failed at pin 7 with a -1025V stress (see Figures 9 and 10).

Next, additional samples of Device A and Device B were tested. During these test, however, the pin-to-ground capacitance element was eliminated by removing tester pogo pins. Device A only included pogo pins for pins 1 to 3 and Device B only included pogo pins for pins 7 and 9. These results indicated Device A now failed at pin 2 with a 925V stress and Device B failed at pin 9 with a -1175V stress (see Figures 9 and 10).

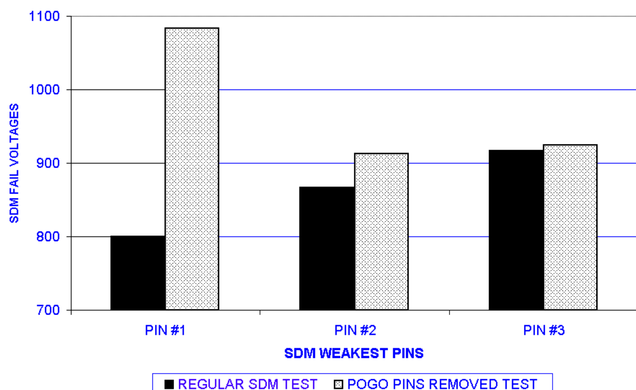

Figure 9: SDM failure threshold levels for Device A; regular SDM testing versus testing with reduced pin capacitance.

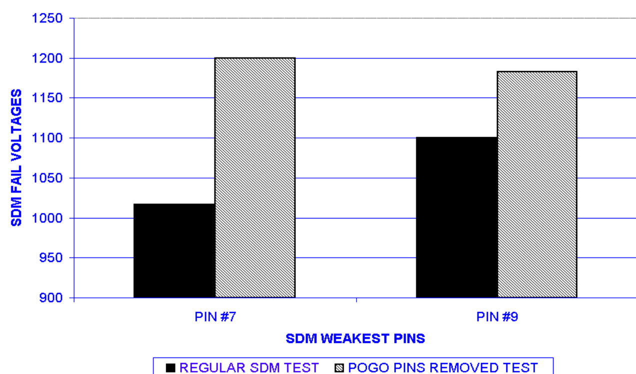

Figure 10: SDM failure threshold levels for Device B; regular SDM testing versus testing with reduced pin capacitance.

Note that in the second experiment Ctt and Cpsps elements are still present between the device pins. However, they do not add to the discharge because there is no voltage across the Ctt elements after pre-charge. The second experiment eliminated the Cpopo and Cb elements (see Figure 4). These experiments indicate that when the SDM test configuration is modified to better simulate real-world CDM events (i.e., little or no capacitive loading at the DUT pins), the threshold voltage level and failing pin changes.

These last results show that the SDM fail voltage for the weakest pin may not actually be the weakest pin. Results have demonstrated that the location and nature of metal trace lines on the test fixture board will determine which device pin receives the greatest SDM stress. The DUT pin receiving this stress is completely arbitrary and is due primarily to the design and layout of the TFB.

VI. Summary and Conclusions

This paper analyzed a commercial SDM tester and determined the important capacitive elements within the test system. Parasitic background capacitance models with various levels of complexity were introduced and measured. We determined that both the pin-to-ground and pin-to-pin capacitance varies widely with the TFB, tester pin count, and socket configuration. In addition, this current generation SDM tester can not detect small capacitance difference due to changes in the package type because of the large DUT pin parasitic background capacitance.

SDM testing on actual integrated circuit devices demonstrated that devices may fail at different pre-charge voltages, and even different device pins, when the tester background capacitance is reduced. This is a serious concern; since the addition of tester background capacitance to a pin under test is merely an artifact of the SDM test system, it is not present in a real-world CDM event.

Current SDM testers have been successfully used by integrated circuit manufacturers to identify CDM-vulnerable pins and make appropriate design changes. However, as the package size and number of socket pins increases, the capability of the SDM tester to detect CDM sensitive pins is reduced. False identification of CDM robust circuits is a real potential problem.

In order to minimize the parasitic elements identified in this paper, an SDM test system should ideally electrically isolate the pins at the test socket. This ***second generation*** "true socket CDM" tester would simply charge the device and nothing more.

The ESD Association Standards Working Group 5.3.2 concludes that it may not be possible to define an SDM tester specification standard. Tester background parasitic elements play such an important role in the SDM discharge event that correlation between test systems built by different manufacturers is unlikely without completely duplicating a particular tester.

Working Group 5.3.2 plans to publish a separate technical report to identify possible work that could be

pursued to overcome some of these issues discussed in this paper. The authors want to encourage work on the development of a second generation SDM test system that eliminates, or at least significantly reduces the parasitics connected to the DUT pin identified during this investigation.

Acknowledgments

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Appendix I:
SDM Test System Description

For the reader who is unfamiliar with the physical construction of the this commercial SDM tester, this Appendix provides a brief additional description. Figure A1 illustrates a short module inserted into a test socket. The socket pins are connected to a relay matrix through a test fixture board (TFB) and a series of pogo pins. The pogo pins make the contact to the test fixture board (which has to be interchangeable to allow for different test sockets to be used). On the TFB, metal trace lines make the connection from the test socket pins to the pogo pin contacts.

The SDM testers used in this study included a 256 pin system (used for 32 to 256 pin evaluations) and a 512 pin system configured to perform as a 256 pin system in addition to a standard 512 pin system (for 32 to 512 pin evaluations). The basic operation of the SDM test system uses a high voltage supply to charge designated

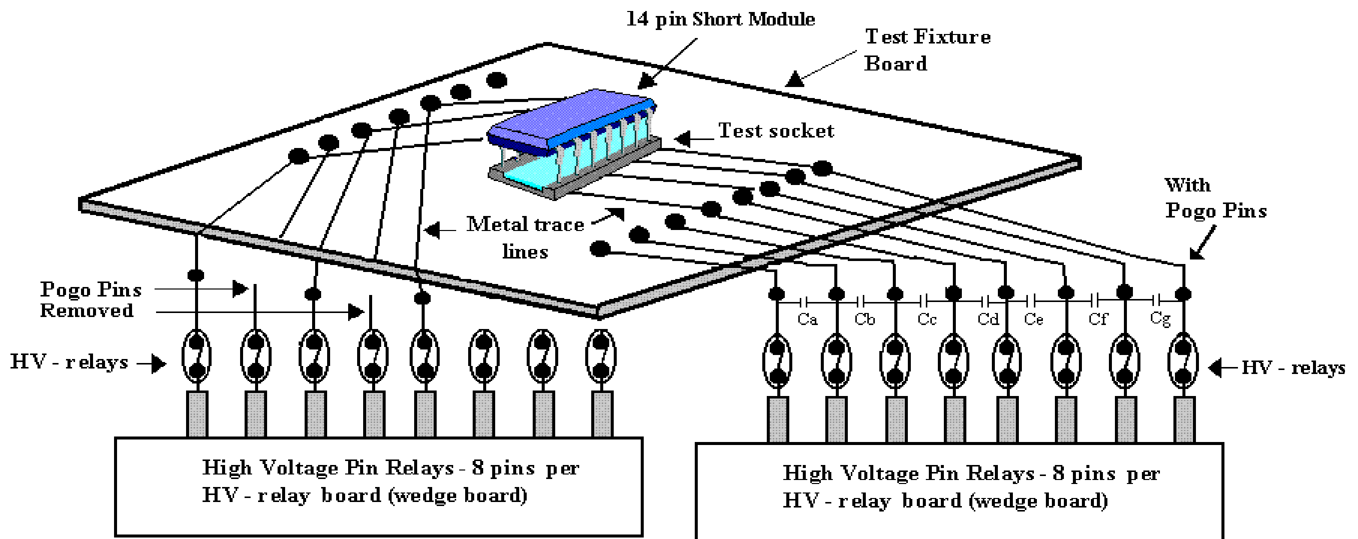

Figure A1: Further details of the commercial SDM tester construction.

device pin(s) in a test socket through a high voltage relay. All remaining device pins in the test socket are floating until a relay-matrix switch for a specific pin under test closes resulting in a device discharge through that pin to ground. In this specific type of SDM test system, different test fixture boards (TFBs) are used for each type of test socket. As a result, each TFB is designed slightly different with varying wire lengths between the high voltage relay (HV-relay) board pogo pins and the TFB socket pins. Each HV-relay board (sometimes referred to as a wedge card) supports eight different socket pins; for a 256 pin test system there are 32 different HV-relay boards. Each HV-relay board is identical and placed radially (see Figure A2).

Figure A3 illustrates how a 512 pin tester is created by essentially connecting two 256 pin testers, including HV supplies and associated HV-relay boards, in parallel. An interface board is placed between the two HV supplies and the test fixture board to create a 512 pin test system. As a result, the wire traces between the HV-relay pogo pins and socket pins are longer than in the single 256 pin tester.

Appendix II: Short Modules and Current Probes

A short module consists of a 14 pin DIL package with all pins shorted internally. One of the external pins is replaced with a 2.5 inch (6.26 cm) wire that can then be inserted through a current probe. The short modules were used two ways: with all module pins inserted into the test socket and rotated 90 degrees so that only two module pins were placed in the test socket (see Figure A4).

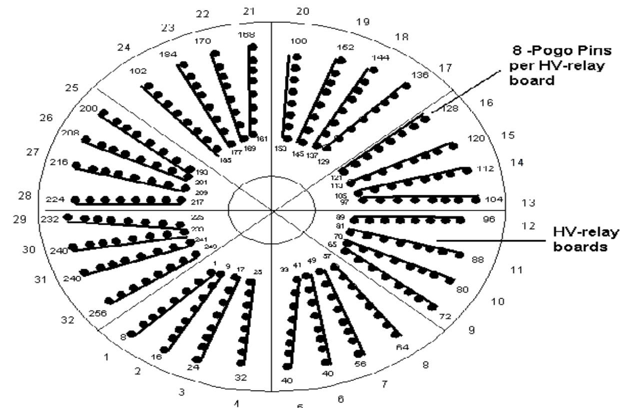

Figure A2: 256 pin SDM test system layout showing location of HV-relay boards (wedge cards) and pogo pins.

To further investigate the SDM calibration module and CT-1 current probe measurements, a prototype fast transient current probe, the KT-2, was used to capture discharge current waveforms (see Figure A5). The CT-1 and KT-2 current probes were characterized using a HP-54120 12.5 Ghz-BW digital sampling oscilloscope with a 35 ps rise time step function as the input signal. According to Barth [15], measurements using this new current probe showed a rise time on the order of 150 ps; and a sensitivity of 8.77 mV/mA as compared to a 5 mV/mA for the CT-1 current probe. The KT-2 had

additional ringing and overshoot of about 20% not present in the CT-1, which did not substantially affect our waveform analysis. We used the KT-2 because our efforts were to obtain the fastest rise time current measurement sensor possible. CDM like discharges require fast rise times and the KT-1 has a 2.3 times faster rise time than the 350 ps rise time of the CT-1 current probe.

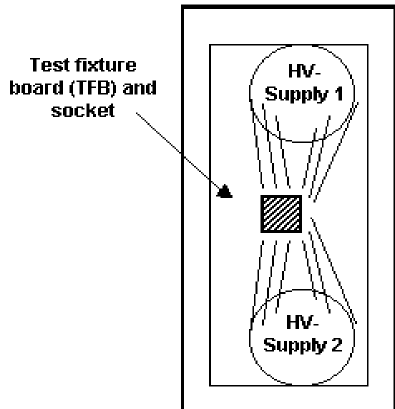

Figure A3: Illustration of a 512 pin test system and placement of two parallel HV supplies.

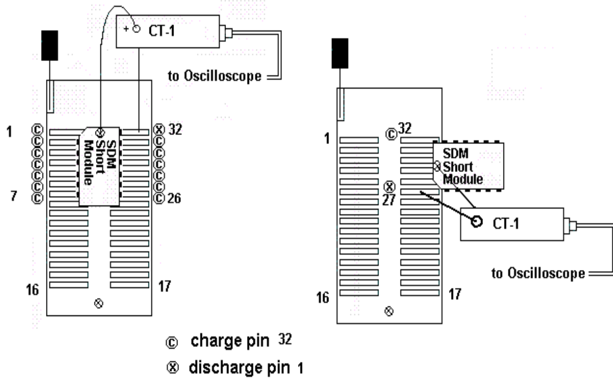

Figure A4: 14 pin short module in a 32 pin socket.

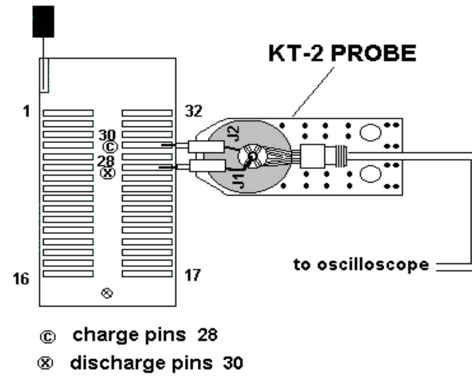

Figure A5: Prototype KT-2 current probe in a 32 pin socket.